FIG. 1
PRIOR ART

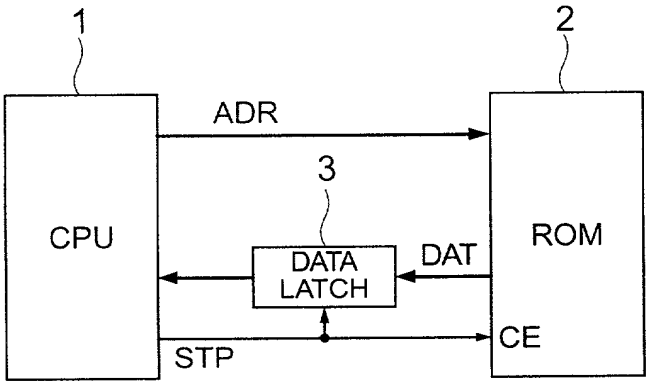


FIG. 2

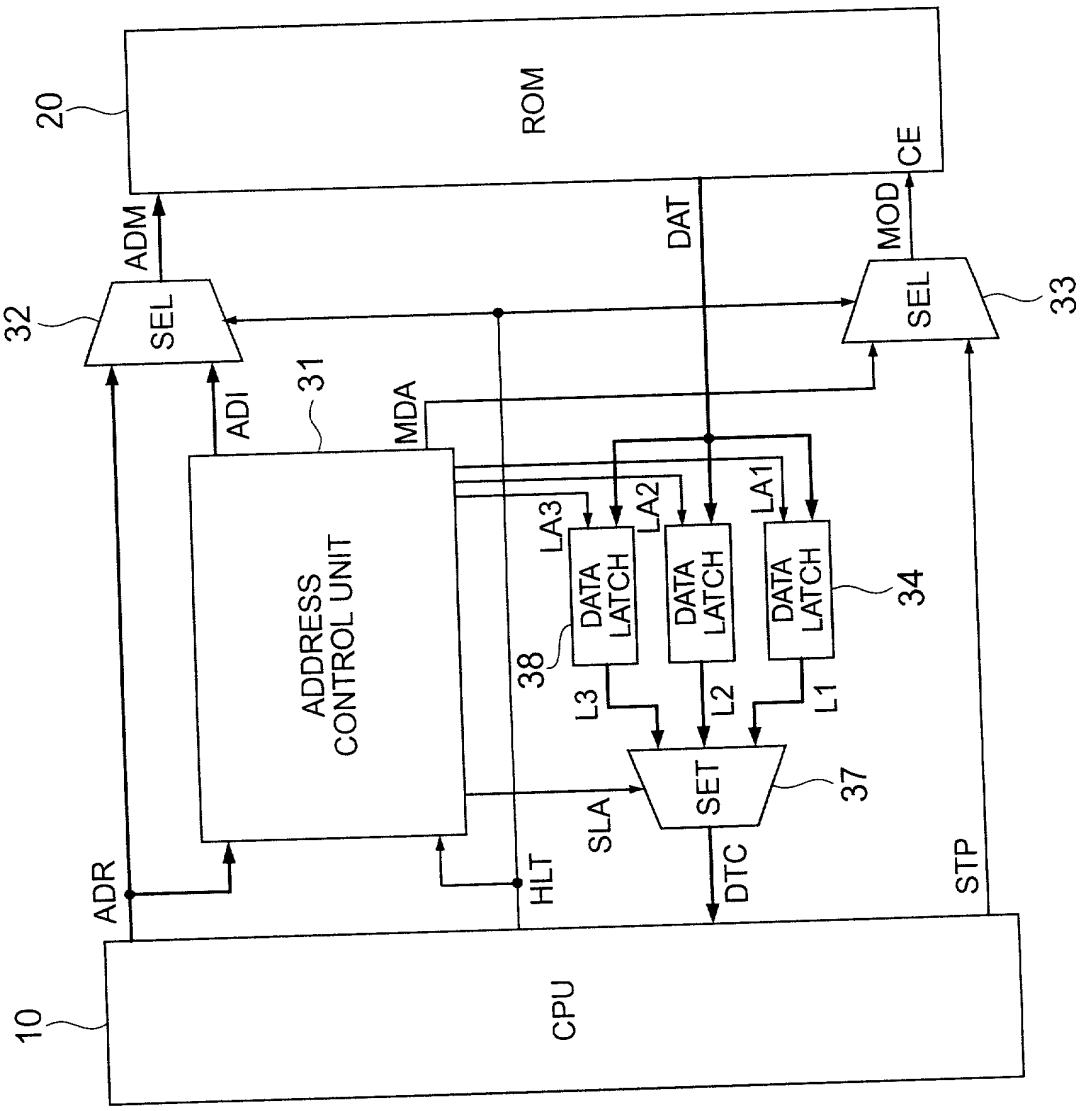

ROM
20
CE
MOD
DAT
ADM
SEL
32
SEL
33
ADI
31
MDA
ADDRESS
CONTROL UNIT
LA3
LA2
LA1
DATA
LATCH
DATA
LATCH
DATA
LATCH
38
34
L3
L2
L1
SET
37
SLA
DTC
STP
HLT
ADR
CPU
10

FIG. 3

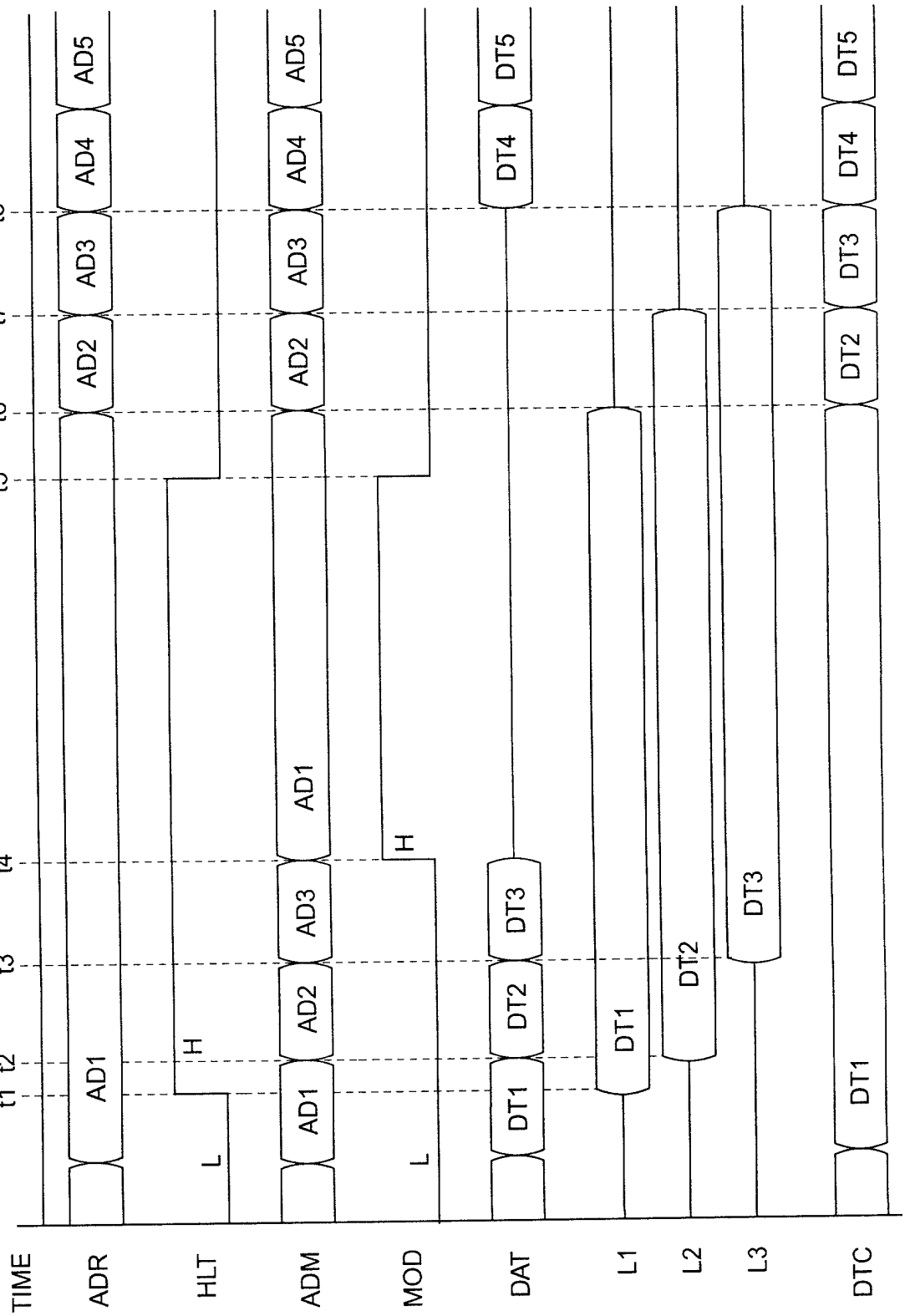

TIME
ADR
HLT
ADM
MOD
DAT
L1
L2
L3
DTC
t1
t2
t3
t4
t5
t6
t7
t8
AD1
AD2
AD3
AD4
AD5
H
L
DT1
DT2
DT3
DT4
DT5

FIG. 4

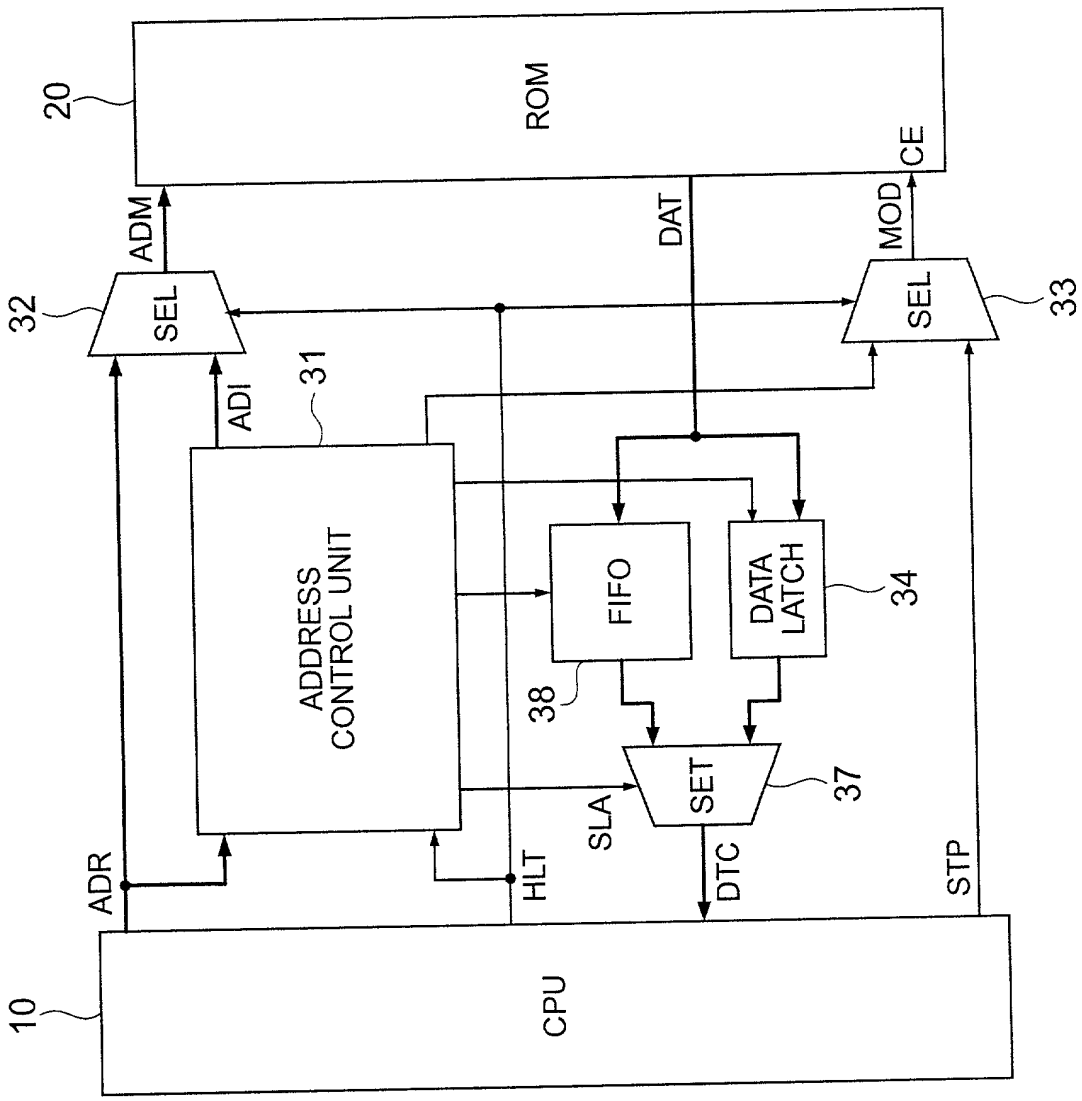

20
ROM
CE
MOD
DAT
ADM
32
SEL
SEL
33
ADI
31
ADDRESS
CONTROL UNIT
FIFO
DATA
LATCH
34
38
SET
37
SLA
DTC
ADR
HLT
STP
10
CPU

FIG. 5

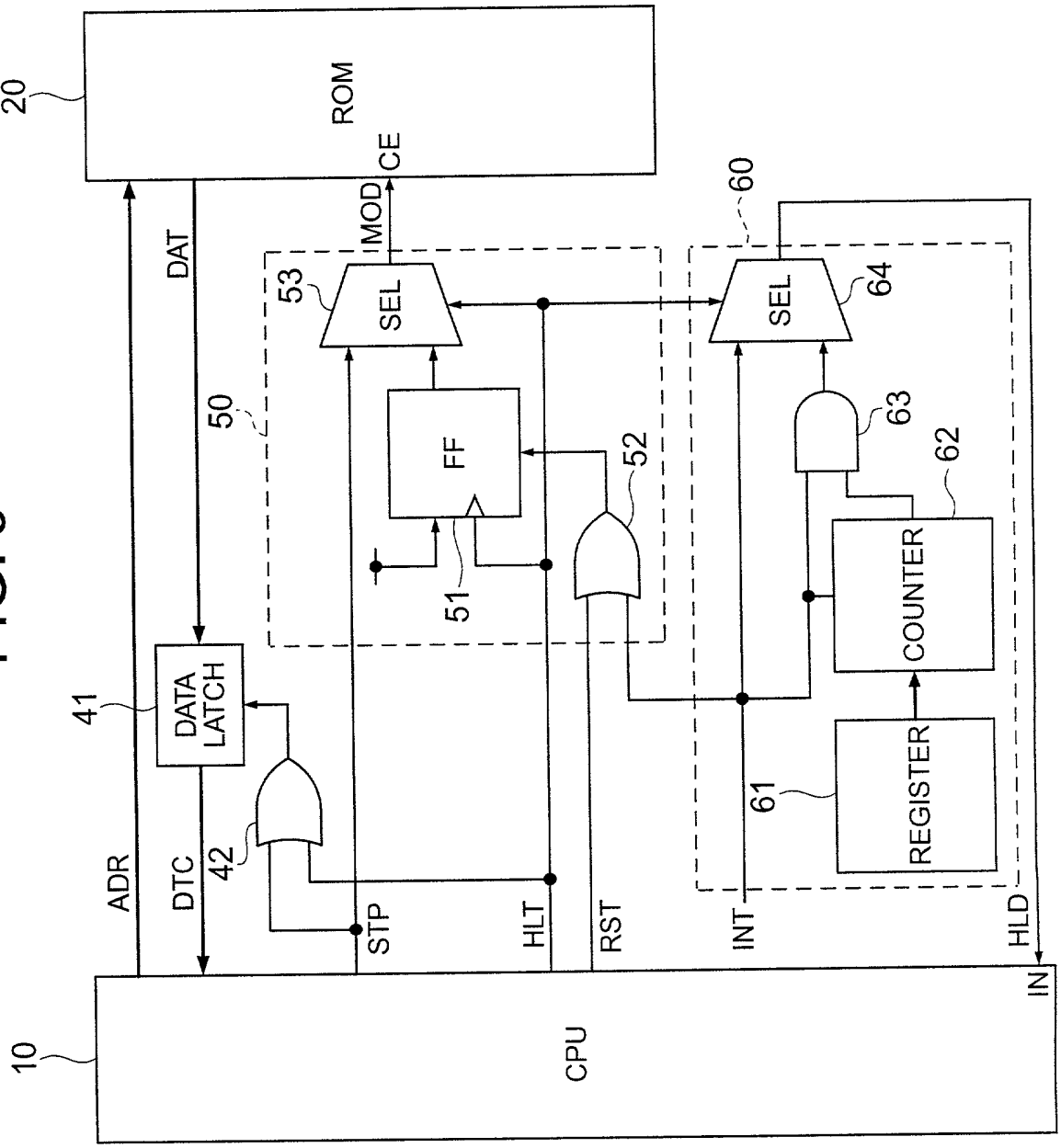

20
ROM
CE
MOD
DAT
60
53
SEL
64
SEL
50
FF
63
52
62
COUNTER
51
41
DATA LATCH
REGISTER
61
ADR
DTC
42
STP
HLT
RST
INT
HLD
IN
10
CPU

FIG. 6

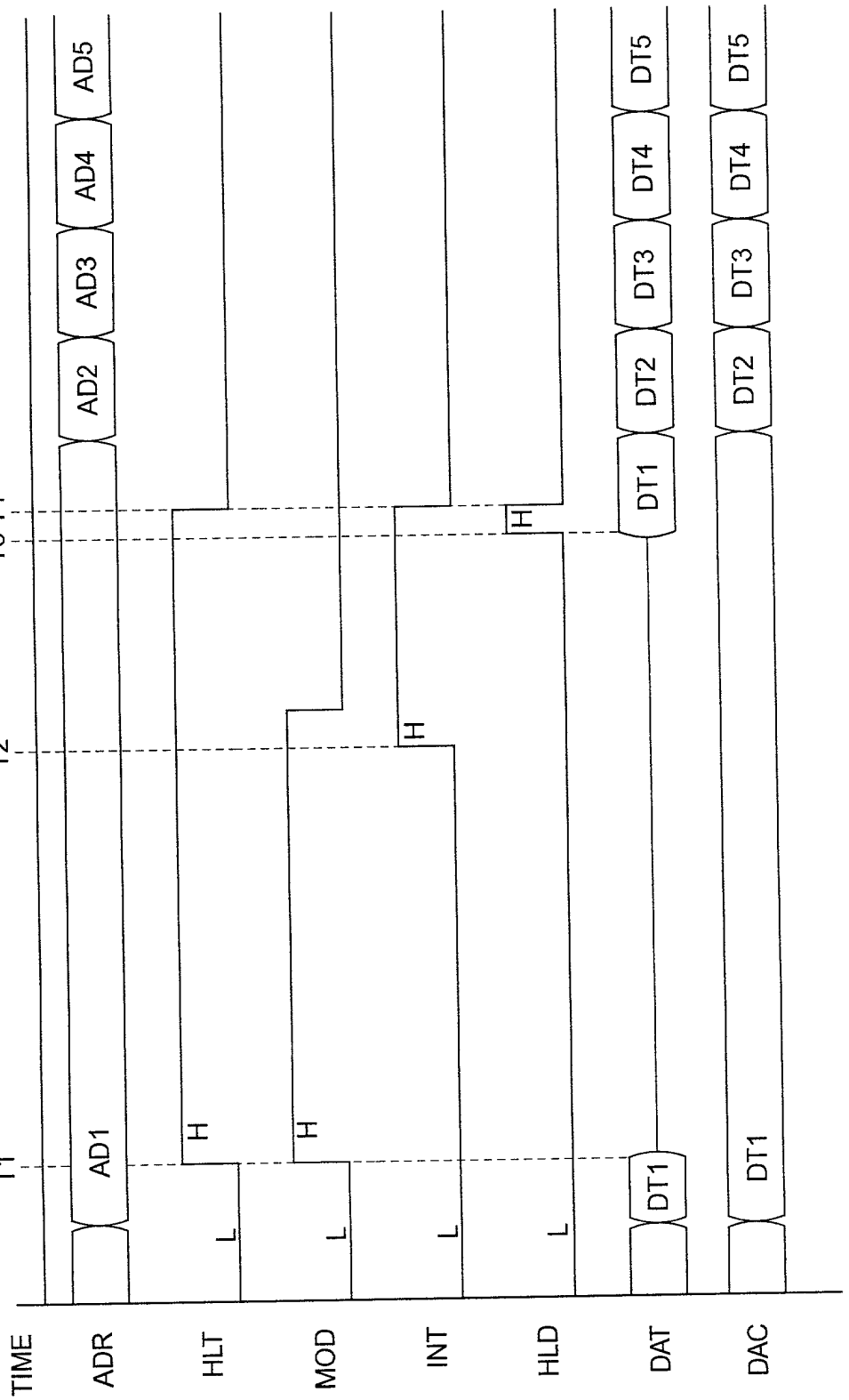

TIME
ADR
HLT
MOD
INT
HLD
DAT
DAC
T1
T2
T3 T4
AD1
AD2
AD3
AD4
AD5
H
L
DT1
DT2
DT3
DT4
DT5

FIG. 7

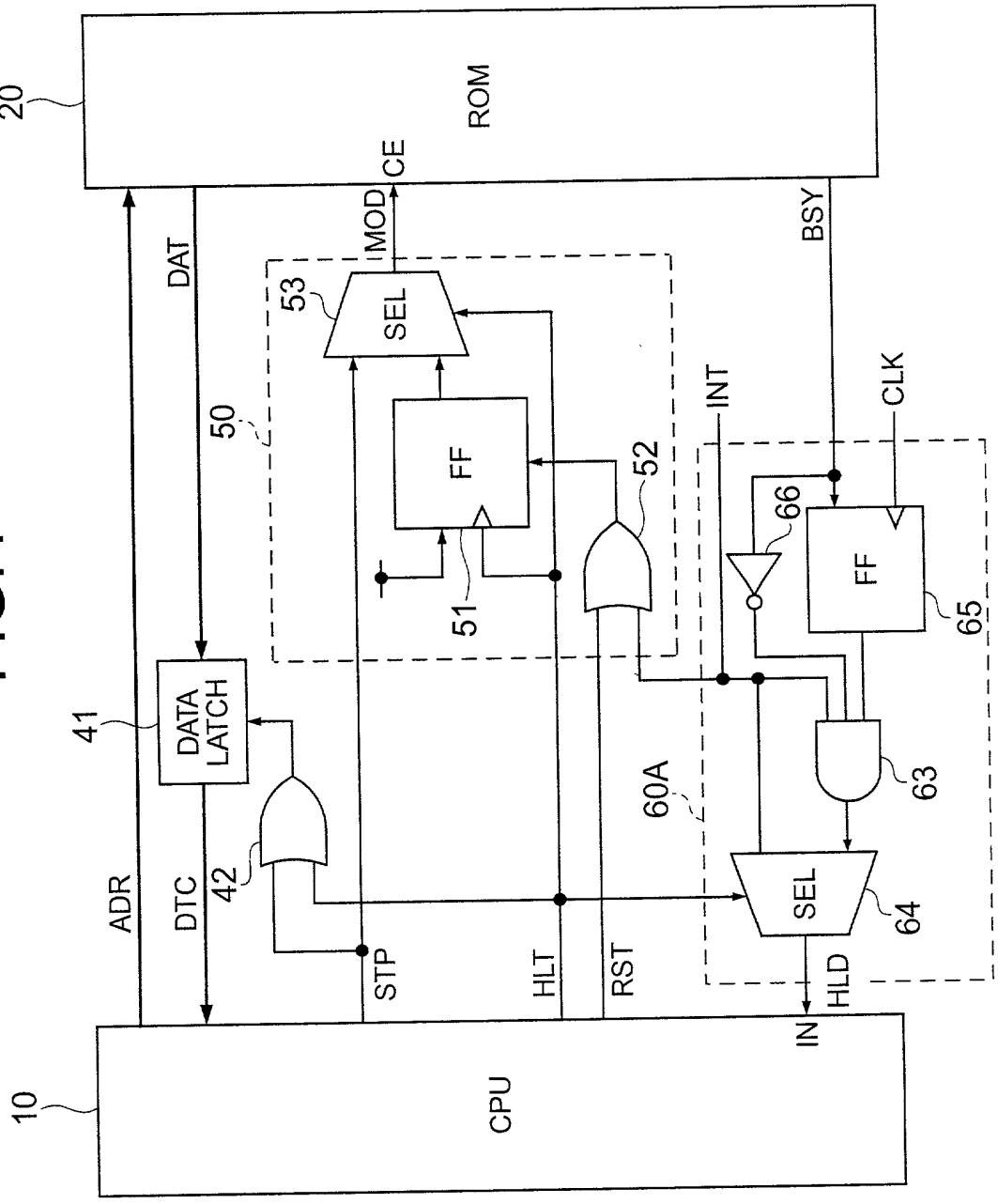
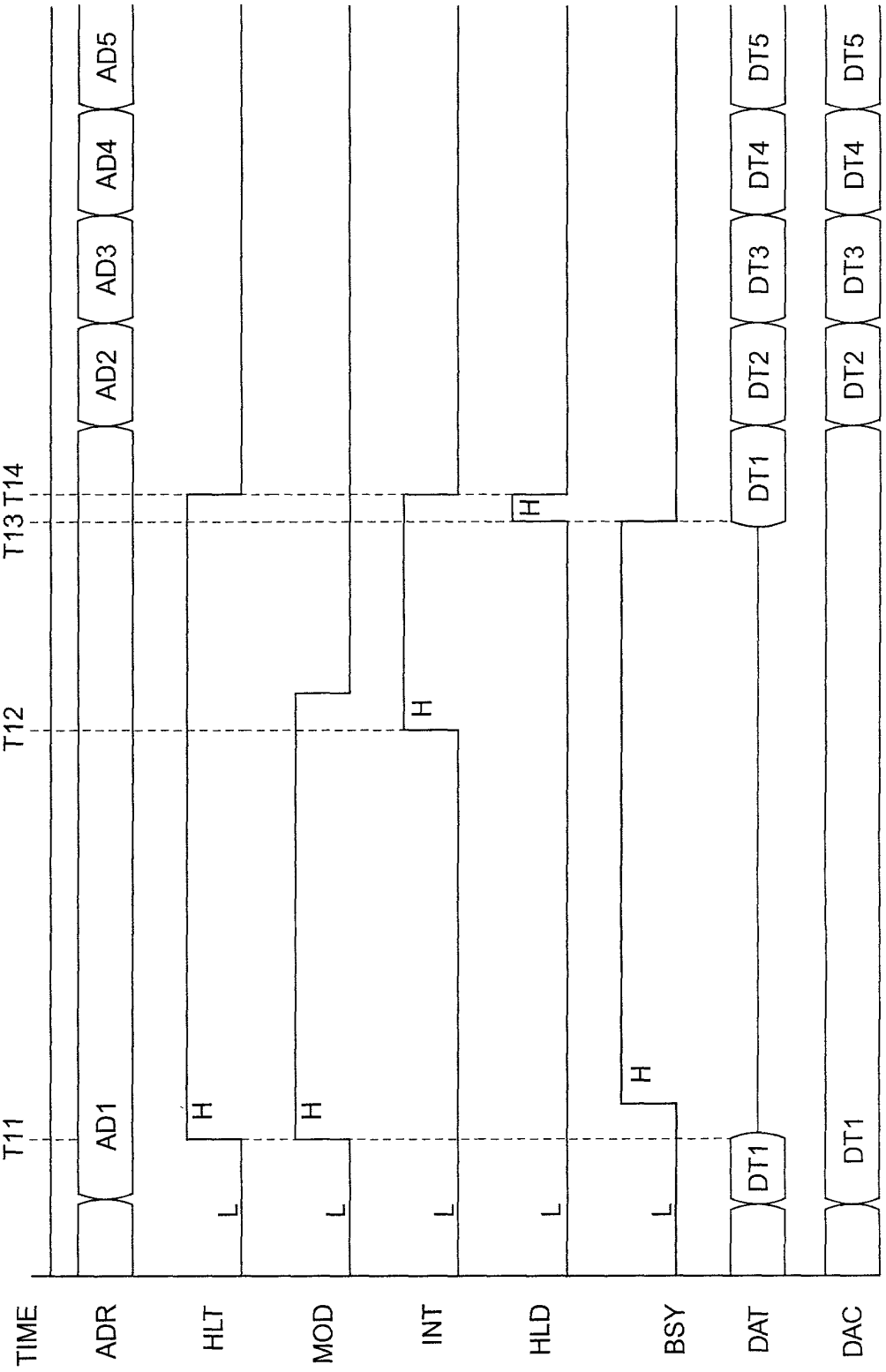

20
ROM
CE
MOD
DAT
BSY
53
SEL
50
FF
52
INT
CLK
66
51
FF
65
41
DATA LATCH
60A
63
ADR
DTC
42
SEL
64
STP
HLT
RST
HLD
IN
10
CPU

FIG. 8


TIME
ADR
HLT
MOD
INT
HLD
BSY
DAT
DAC
T11
T12
T13
T14
AD1
AD2
AD3
AD4
AD5
DT1
DT2
DT3
DT4
DT5
H
L